IN THE CLAIMS

1. (currently amended) A transceiver system for receiving content contained in a secure digital broadcast signal, comprising:

a first component for generating a data stream;

a first encryption unit coupled to the first component, and for encrypting the data stream for transmission to generate an encrypted data stream;

a second component for generating a video signal for a display device;

a second encryption unit coupled to the second component and for decrypting the encrypted data stream received from the first component;

a bi-direcitonal digital bus coupled to the first encryption unit and the second encryption unit; and

a third component coupled to the bus for arbitration such that content from the data stream is securely transferred across the bus and without exposing an unencrypted data stream.

2. (original) The system of Claim 1 wherein the transceiver is a set-top box.

3. (original) The system of Claim 1 wherein the first component is an audio video decode block for decoding the data stream from a digital broadcast signal.

4. (original) The system of Claim 1 wherein the second component is a graphics block for generating the video signal from the data stream received from the first component.

5. (original) The system of Claim 1 wherein the third component is a CPU (central processing unit) block coupled to the bus for managing an encryption process of the first encryption unit and the second encryption unit.

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6. (original) The system of Claim 5 wherein the encryption process is key-based encryption process and the CPU block manages the distribution of keys to the first encryption unit and the second encryption unit.

7. (original) The system of Claim 5 further comprising an arbiter coupled to the CPU block for arbitration of the bus.

8. (original) The system of Claim 1 wherein the first component, second component, and third component include respective identification registers for identifying each component.

9. (original) The system of Claim 1 wherein said data stream is encrypted using an encryption process substantially compliant with DES ECB (Data Encryption Standard Electronic Code Book).

10. (original) The system of Claim 1 wherein the bus is a PCI (Peripheral Component Interconnect) compliant bus and each encryption unit performs encryption and decryption.

11. (original) The system of Claim 1 further comprising a front end block coupled to the bus for receiving the digital broadcast signal and generating the data stream therefrom, the first component coupled to receive the data stream from the front end block via the bus.

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12. (original) The system of Claim 1 wherein the data stream is substantially compliant with a version of the MPEG (Moving Pictures Experts Group) format.

13. (currently amended) In a set-top box transceiver, a high security bus architecture for implementing secure transmission of data between components of the transceiver, comprising:

a bus;

a first encryption unit coupled to the bus for encrypting a data stream to generate an encrypted data stream, the data stream received from a first component;

a second encryption unit coupled to the bus for decrypting the encrypted data stream received from the first encryption unit via the bus, the data stream for transmission to a second component; and

a third component coupled to the bus for arbitration of the bus to coordinate transmission of the encrypted data stream from the first encryption unit to the second encryption unit such that content from the data stream is securely transferred across the bus and without exposing an unencrypted data stream.

14. (original) The architecture of Claim 13 wherein the first component and the first encryption unit are built into a first integrated circuit device and the second component and the second encryption unit are built into a second integrated circuit device.

15. (original) The architecture of Claim 13 wherein the first component is an audio video decode block for decoding the data stream from the external source.

16. (original) The architecture of Claim 13 wherein the second component is a graphics block for generating a video signal from the data stream received from the first component.

17. (original) The architecture of Claim 13 wherein the first component is a conditional access block for descrambling the digital broadcast signal.

18. (original) The architecture of Claim 13 wherein the second component is an audio video decode block for decoding the data stream received from the first component.

19. (original) The architecture of Claim 13 wherein the third component is a CPU (central processing unit) block coupled to the bus for managing an encryption process of the first encryption unit and the second encryption unit.

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20. (original) The architecture of Claim 19 wherein the encryption process is key-based encryption process and the CPU block manages the distribution of keys to the first encryption unit and the second encryption unit via the bus.

21. (original) The architecture of Claim 19 further comprising an arbiter coupled to the CPU block for arbitration of the bus.

22. (original) The architecture of Claim 19 wherein the first component, second component, and third component include respective identification registers for implementing component identification via the bus.

23. (original) The architecture of Claim 19 wherein said data stream is encrypted using an encryption process substantially compliant with DES ECB (Data Encryption Standard Electronic Code Book).

24. (original) The architecture of Claim 19 wherein the bus is a PCI (Peripheral Component Interconect) compliant bus and provides bi-directional communication between the first component and the second component.

25. (currently amended) In a transceiver for receiving a digital broadcast signal, a method for implementing secure transmission of data from the digital broadcast signal between internal components of the transceiver via a bus, the method comprising the steps of:

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a) accessing a digital broadcast signal using a first component of a transceiver;

b) generating a data stream by descrambling the digital broadcast signal using the first component;

c) encrypting the data stream using a first encryption unit to generate an encrypted data stream;

d) transmitting the encrypted data stream to a second component via a bus; and

e) decrypting the data stream using a second encryption unit coupled to the second component such that the bus carries only an encrypted version of the data stream and without exposing an unencrypted data stream.

26. (original) The method of Claim 25 wherein the transceiver is a set-top box.

27. (original) The method of Claim 25 wherein the bus is a PCI (Peripheral Component Interconect) compliant bus and provides bi-directional communication between the first component and the second component.

28. (original) The method of Claim 25 further comprising the step of decoding the data stream from the external source using an audio video decode block.

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29. (original) The method of Claim 25 further comprising the step of generating a video signal from the data stream received from the first component using a graphics block.

30. (original) The method of Claim 25 further comprising the step of managing an encryption process of the first encryption unit and the second encryption unit using a CPU (central processing unit) block coupled to the bus.

31. (original) The method of Claim 30 wherein the encryption process is key-based encryption process and the CPU block manages the distribution of keys to the first encryption unit and the second encryption unit.

32. (original) The method of Claim 25 wherein said data stream is encrypted using an encryption routine substantially compliant with DES ECB (Data Encryption Standard Electronic Code Book).

33. (original) The method of Claim 25 wherein the data stream is substantially compliant with a version of the MPEG (Moving Pictures Experts Group) format.

34. (currently amended) A bus architecture for a digital transceiver comprising:

a high speed bi-directional bus for communicating digital information thereon;

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a first encryption/decryption unit (EDU) coupled to the bus for providing decrypted digital signals to a first functional unit from the bus and for providing encrypted digital signals to the bus from the first functional unit;

a second EDU coupled to the bus for providing decrypted digital signals to a second functional unit from the bus and for providing encrypted digital signals to the bus from the second functional unit; and

a controller for controlling transmission of digital signals on the bus wherein audio video signals are transmitted between the first and second EDUs in encrypted form, the controller also for establishing encryption/decryption keys for the first and second EDUs and without exposing an unencrypted data stream.

35. (original) The architecture of Claim 34 wherein the first functional unit is an audio video decode block for decoding a data stream from a digital broadcast signal.

36. (original) The architecture of Claim 34 wherein the second functional unit is a graphics block for generating a video signal from the audio video digital signals received from the first functional unit.

37. (original) The architecture of Claim 34 wherein the controller is a CPU.

38. (original) The architecture of Claim 34 wherein the encryption process is key-based encryption process and the controller manages the distribution of keys to the first encryption unit and the second encryption unit.

39. (original) The architecture of Claim 34 further comprising an arbiter coupled to the controller for arbitration of the bus.

40. (original) The architecture of Claim 34 wherein the first functional unit, second functional unit, and third functional unit include respective identification registers for identifying each functional unit.

41. (original) The architecture of Claim 34 wherein the audio video digital signals are encrypted using an encryption process substantially compliant with DES ECB (Data Encryption Standard Electronic Code Book).

42. (original) The architecture of Claim 34 wherein the bus is a PCI (Peripheral Component Interconnect) compliant bus.

43. (original) The architecture of Claim 34 further comprising a front end block coupled to the bus for receiving a digital broadcast signal and generating the audio video digital signals therefrom, the first functional unit coupled to receive the audio video signals from the front end block via the bus.

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44. (original) The architecture of Claim 34 wherein the audio video digital signals are substantially compliant with a version of the MPEG (Moving Pictures Experts Group) format.